

GIST has accelerated the development of next-generation devices by up to 100 times... accelerating semiconductor simulations that previously took days

- Professor Sung-Min Hong's research team from the Department of Electrical Engineering and Computer Science has developed a new algorithm that rapidly predicts complex next-generation semiconductor devices in a virtual environment... Simulation speeds, previously taking hours or days, are reduced by 10-100 times
- Combining "quasi-1D modeling (simple channel-direction calculations)" and "regional structural analysis (optimal calculations by dividing the device into sections)" allows for rapid estimation of initial calculation values... Efficiency, accuracy, and stability are ensured without the need for pre-trained AI models
- Flexible application to various device structures. Published in the international journal 《Communications Engineering》



▲ (From left) Professor Sung-Min Hong of the Department of Electrical Engineering and Computer Science at GIST, and researchers Kwang-Woon Lee, In Ki Kim, Seung-Woo Jung, and Min-Seo Jang

The Gwangju Institute of Science and Technology (GIST, President Kichul Lim) announced that a research team led by Professor Sung-Min Hong of the Department of Electrical Engineering and Computer Science has developed a new algorithm that dramatically improves the computational efficiency of semiconductor device simulation, enabling performance predictions of next-generation devices up to 100 times faster than existing methods.

This achievement is significant in that it fundamentally resolves the issue of "long-term simulation," a major obstacle in semiconductor device research and development (R&D).

* semiconductor device simulation: A technology that numerically reproduces and analyzes the electrical and physical behavior of semiconductor devices in a virtual environment. By predicting device behavior, such as current flow, electric field distribution, and heat generation characteristics, prior to actual fabrication, it significantly improves performance optimization and design efficiency. It is generally utilized as a core tool in the field of Technology Computer-Aided Design (TCAD).

To predict and optimize the performance of semiconductor devices, "TCAD simulation*" is essential. TCAD is a technology that precisely predicts the electrical characteristics of a device by numerically calculating the movement of electrons and holes and the distribution of electric fields within the semiconductor, based on physical laws.

However, complex next-generation devices, such as the latest gate-all-around (GAA)* structure and complementary field-effect transistor (CFET)*, require three-dimensional calculations, requiring

simulations that can take hours or even days. This has significantly slowed down research and development.

* TCAD simulation (Technology Computer-Aided Design simulation): A technology that simulates the electrical and physical characteristics of semiconductor devices using a computer, enabling performance prediction and optimization without the need for actual device fabrication. It numerically calculates the movement of electrons and holes, electric field distribution, and charge accumulation within a semiconductor based on physical laws. This allows for precise analysis of key device operating characteristics, such as current-voltage characteristics, switching speed, and leakage current.

* gate-all-around (GAA): A semiconductor transistor structure in which the gate completely surrounds the channel. Unlike conventional planar transistors, where the gate controls only a portion of the channel, GAA transistors have a gate that wraps 360 degrees around the channel, allowing for more precise control of current flow, reducing leakage current and improving performance. This structure has recently attracted attention for the implementation of highly integrated, low-power transistors in next-generation semiconductor devices, particularly those using 3nm and below processes.

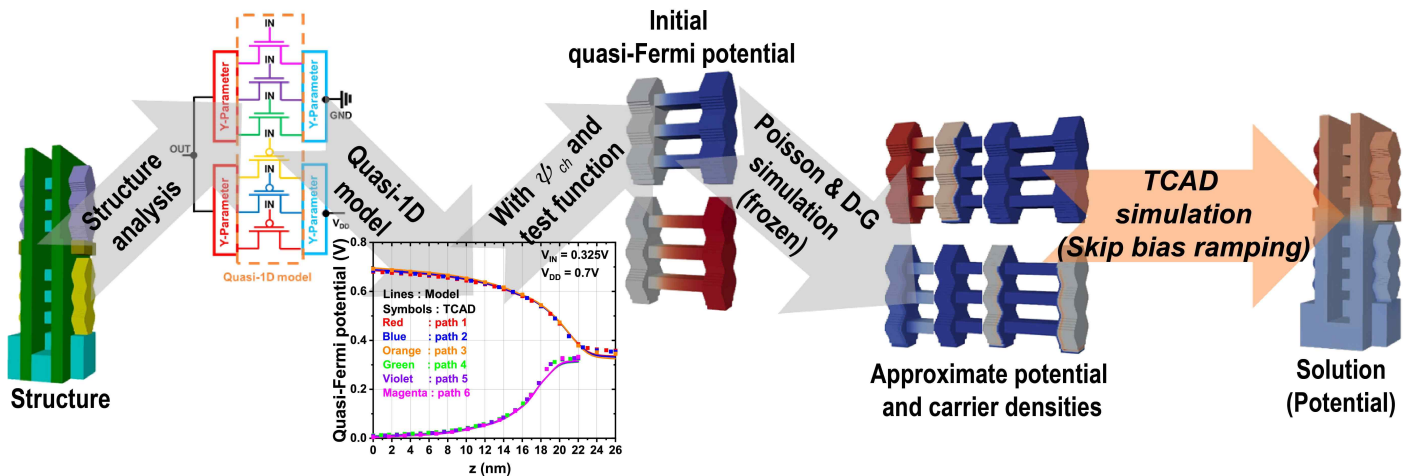
* CFET (Complementary FET): A next-generation semiconductor device architecture. Instead of arranging n-type (NMOS) and p-type (PMOS) transistors side by side in a plane like conventional CMOS, it stacks them vertically to maximize integration. This allows for more devices to be integrated within the same area, simultaneously improving circuit performance and power efficiency. It is attracting attention as a promising alternative for ultra-fine processes below 1nm.

In particular, the "bias ramping" process, which gradually increases the voltage to induce convergence, was essential for stable calculations under the desired voltage conditions. This process accounted for the majority of the overall calculation time and acted as a bottleneck.

Recent attempts have utilized trained artificial neural networks (ANNs) to generate superior initial estimates and reduce unnecessary intermediate steps. However, applying these techniques to new structures requires additional data and training, significantly limiting their immediate application in industrial settings.

* bias ramping: When simulating semiconductor devices or circuits, this process involves gradually increasing the voltage or current, rather than applying it all at once. This allows for more stable simulation calculations when solving nonlinear equations.

To address this issue, the research team proposed a new approach that combines "quasi-1D modeling*" and "region-wise structure analysis*." This method can significantly reduce semiconductor device simulation time without requiring a pre-training process.

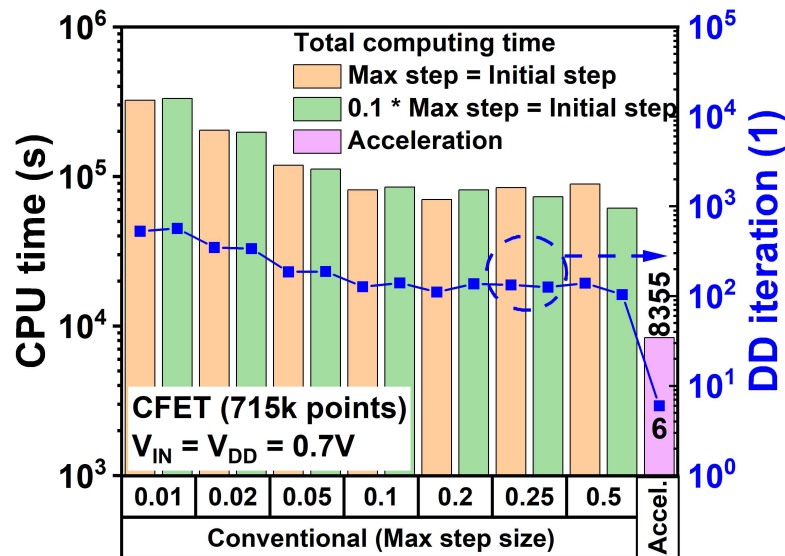


▲ Overall schematic of the proposed method. Given a CFET inverter structure, a region-wise structure analysis is performed, followed by a quasi-1D model. The initial estimates are reconstructed into a 3D structure, and the simulation is performed immediately at the desired voltage.

The key is to simplify complex semiconductor devices into a one-dimensional model along the current channel direction, quickly estimating initial solutions. The device is then divided into multiple sections with optimized physical models applied to each section. This omits the previously required bias ramping process while achieving computational speeds 10 to 100 times faster.

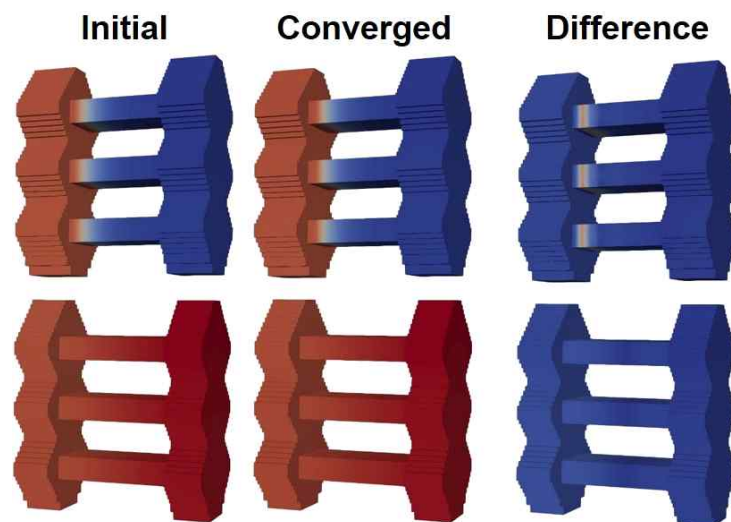
* quasi-1D modeling: This method simplifies complex three-dimensional semiconductor devices and treats them as one-dimensional models along the current channel direction. This allows for rapid initial solution estimation and significantly improves the stability and speed of subsequent precision calculations. Compared to conventional three-dimensional simulations, this method reduces computational burden, dramatically improving simulation speed.

* region-wise structure analysis: This method divides semiconductor devices into multiple sections and applies physical models tailored to the characteristics of each region. Rather than calculating the entire complex device at once, the proposed method performs optimized analyses for each region, ensuring both computational efficiency and accuracy. Its particular advantage lies in its flexibility for application to next-generation devices with diverse structures.



▲ Simulation speed comparison between the existing and proposed methods for a CFET inverter. The comparison is based on total computation time (CPU time) and the number of calculations (DD iterations). Compared to the optimal results of the existing method, the proposed method achieves a 7x reduction in computation time and a 17x reduction in the number of calculations.

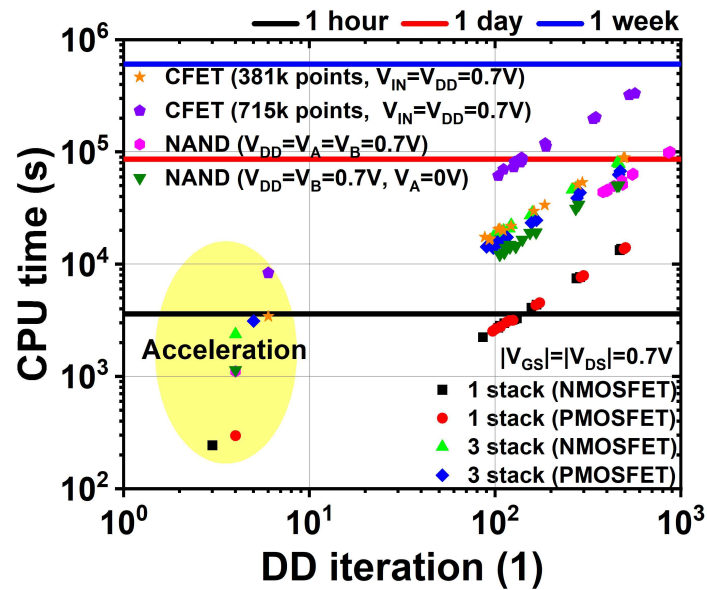
The research team validated the new algorithm on various next-generation devices, including gate-all-around (GAA) devices and complementary CFET inverters.



▲ Comparison of the initial quasi-Fermi potential of a pseudo-1D model (left) and the converged quasi-Fermi potential from a semiconductor device simulation (middle). The difference between the two results (right) is less than 0.1 V, making it an excellent initial estimate.

As a result, simulation speeds are 10 to 100 times faster than conventional methods. Furthermore, the error in key electrical characteristics, such as the voltage transfer characteristics (VTC), compared to conventional TCAD results is kept below 0.1 V, demonstrating high accuracy. Furthermore, consistent results are achieved without performance degradation even when the device geometry (geometric

structure) or mesh conditions (mesh conditions, which refer to the sub-regions divided during the calculation process) change. This demonstrates its stable applicability across a variety of environments and structures.



▲ Comparison of simulations between the existing and proposed methods across various device structures. Even without the use of a trained artificial neural network, a nearly 10-fold reduction in time is observed across a variety of structures.

Professor Sung-Min Hong stated, "This study demonstrates that semiconductor device simulation times can be significantly reduced across a variety of structures without the need for a pre-trained artificial neural network-based AI model." He added, "The efficiency, accuracy, and stability of the proposed technique will contribute to accelerating the development of next-generation semiconductor devices and enhancing research efficiency."

This research, supervised by Professor Sung-Min Hong of the Department of Electrical Engineering and Computer Science at GIST and conducted by researchers Lee Kwang-Woon Lee, In Ki Kim, Seung-Woo Jung, and Min-Seo Jang, was supported by the Ministry of Science and ICT and the National Research Foundation of Korea through the Individual Basic Research Program (Medium-Career). The results were published online in the international journal 《Communications Engineering》 on September 25, 2025.

Meanwhile, GIST stated that this research achievement considered both academic significance and industrial applicability, and that technology transfer inquiries can be made through the Technology Commercialization Center (hgmoon@gist.ac.kr).