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Hybrid Complementary Logic Circuits of One-Dimensional Nanomaterials with Adjustment of Operation Voltage

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The continued miniaturization of electronics through the top-down approach is expected to reach fundamental physical limits and, thus, has motivated significant efforts toward the development of new functional materials and devices based on nanoscale building blocks.[1–8] In particular, carbon nanotubes (CNTs) and ZnO nanowires are promising candidates for diverse applications in nanoelectronics, because they can function as the semiconductor channels with fascinating electrical transport properties for electronic devices including diodes,[9] field-effect transistors (FETs),[4,10–12] and circuits.[9,13,14] In spite of the demonstrated ability to achieve the superior device performance in their individual single devices, a wide variability in the on-state current and voltage, resulting from the inability of complementary doping to precisely and equally modulate their electrical properties, has been one of the major obstacles to implementing high-performance complementary logic circuits for more practical applications.[15–17] A potential solution to go beyond the limits and functionality of individual single devices for the desirable logic circuits is a hybrid approach, which enables us to take each advantageous property of hybrid nanomaterials as electronic components for the realization of functional nanoelectronics.

In our study, p-type single-walled carbon nanotubes (SWNTs) and n-type ZnO nanowires with excellent and reliable electrical properties have been used for a complementary circuit design, such as a complementary inverter, NOR and NAND logic gates, and a static random-access memory (SRAM) cell with operation superior to devices and circuits based on a single-carrier type and/or diodes.[9,13,18–20] Our hybrid complementary devices can be configured in an efficient circuit architecture to decrease the power dissipation and to increase logic performance without additional compensation circuits. To this end, the precise modulation and matching of the current and operating voltage in transistors have been achieved electrostatically by adjusting the population of proton radiation-generated charges in the dielectric layer, providing an alternative to chemical doping. Recently, we have demonstrated that SWNT FETs show a high tolerance against proton radiation,[21] while the electrical characteristics of ZnO-nanowire FETs are sensitively influenced by the surface trap states at the interface between the ZnO nanowires and dielectric layer.[11,22] Here, we report a new layout of predictable and controllable complementary logic circuits based on hybrid nanodevices comprising p-channel SWNT and n-channel ZnO nanowire transistors, providing a hybrid approach to combine advantageous characteristic functions for the modulation of the current and operating voltage in transistors through proton radiation-generated charges, which allow a simple way to design favorable logic circuits.

Figure 1a shows the layout of our inverter devices integrated by hybrid complementary FETs (see Fig. S1 of the Supporting Information). p-type SWNT and n-type ZnO nanowire FETs were used to assemble various logic devices. In each configuration of the logic circuit structures, the SWNT FETs have a network structure of CNTs (inset of Fig. 1, right bottom) in order to provide sufficient current output overcoming the limited current-carrying capacity of individual SWNTs,[23,24] enabling the current match with the ZnO-nanowire FET device[25] (inset of Fig. 1, left bottom). Another advantage of the network SWNT devices is that the statistical averaging effects can lead to a small device-to-device variation in the electrical properties[23,26] (see Fig. S2 of the Supporting Information). The circuit devices were then irradiated with proton beams in order to adjust the threshold voltage of transistors via the proton-generated charges in the dielectric layer. Figure 1b shows a series of optical images of the complementary inverters composed of n-channel ZnO nanowires and p-channel SWNT-network FET devices. From left to right, the zoomed-in pictures show our mask patterned image, device sizes, and structures.

Figure 2a shows the output characteristics of the *n*-channel ZnO nanowire FET before and after proton irradiation with a fluence of $1 \times 10^{11}\,\mathrm{cm}^{-2}$. It is observed that the current through the channel of a ZnO nanowire before and after proton irradiation is proportional to the applied drain bias within the linear regime at low bias. It changes little by applied gate bias in the saturation regime at high bias, indicating typical electrical behavior of n-type FETs. Here, an interesting finding is that the electrical conductance and threshold voltage can be modulated predictably

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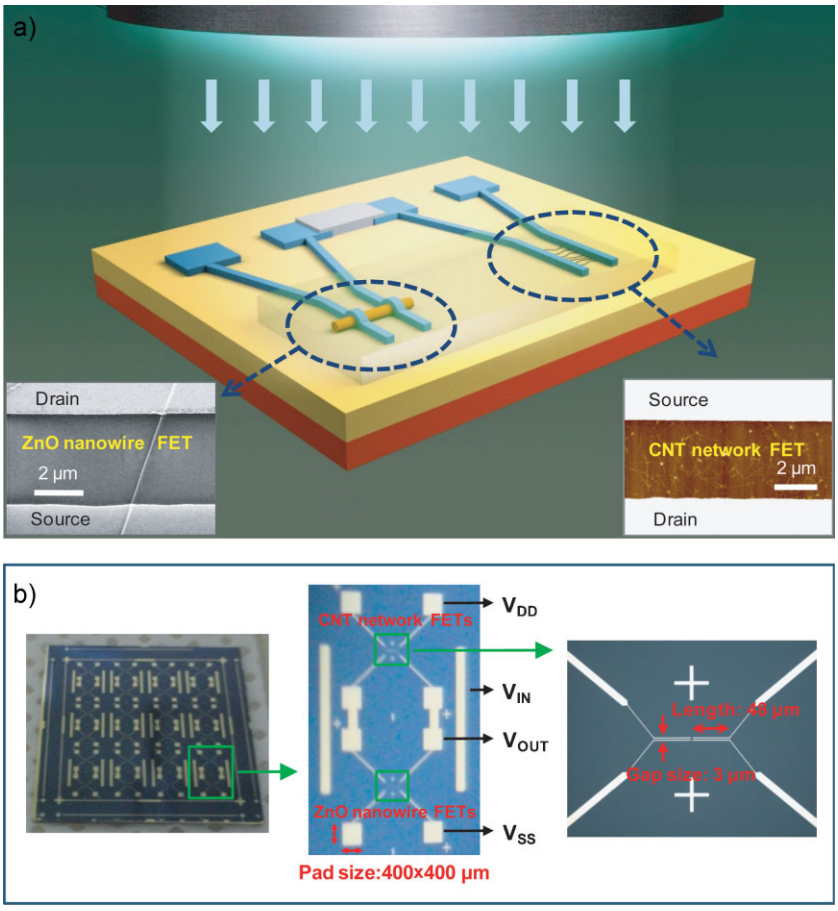

Figure 1. a) Device layout of the hybrid complementary logic circuit comprising n-channel ZnO nanowire and p-channel SWNT-network FET devices. The circuit devices were irradiated with proton beams with energy of 10 MeV and fluences of 1×10^{11} and 1×10^{12} cm^{-2}, which correspond to total absorbed dose of 64.1 and 641 krad and exposure time of 600 and 6000 s, respectively. Inset: atomic force microscopy image of an SWNT-network FET (right bottom) and field-emission scanning electron microscopy image of a ZnO-nanowire FET (left bottom). b) Optical images of the hybrid complementary inverters composed of n-channel ZnO nanowire and p-channel SWNT-network FET devices.

by proton radiation as shown in Figure 2a and b. This implies that we can positively shift the threshold voltage of ZnO-nanowire transistors to decrease the power dissipation of complementary logic devices, acting as a fully n-type transistor, where it is ON for positive gate bias and OFF for negative gate bias. Statistically, an average shift of 2.19 V in the threshold voltage was obtained from 52 devices of ZnO-nanowire FETs measured after proton irradiation with a fluence of $1 \times 1011\,cm^{-2}$ (see the detail statistical data in Fig. S3 in the Supporting Information.) It should be noted that the threshold voltage shifts further to more positive values as the dose of proton radiation is increased (Fig. S6, Supporting Information). This suggests that we can control the threshold voltage of ZnO-nanowire FETs through the tuning of built-in potential by radiation-generated charges in the dielectric layer, since the electrical behavior of ZnO-nanowire FETs is strongly affected by the surface-barrier potential.[11,22] The positive shift of threshold voltage is attributed to radiation-induced negative charges trapped at the ZnO-nanowire/SiO_2 interface, causing the carrier depletion in the n-channel ZnO nanowire (a higher gate voltage is required to have the same accumulation channel). In contrast, the p-channel SWNT-network FET devices, showing no significant change in the electrical properties after proton radiation exposure (Fig. 2c and d), are highly resistant against proton beams,[21] and have much less influence on surface-potential changes induced by the trap states formed at the CNT/SiO_2 interface.[27,28] In this context, it is significantly important to match the threshold voltage for less power consumption and the desirable switching behavior in complementary logic circuits.[29,30]

The ability to precisely modulate conductance and threshold voltage of n- and p-channel FETs enables the assembly of a high-performance complementary inverter, which is a basic logic element for realizing all other logic gates. As shown in Figure 3a, we adjusted the threshold voltage of hybrid FETs with a large on–off ratio through proton radiation to allow only electron and hole conductance for positive and negative gate bias, respectively. Before proton radiation, the output voltage (V_{OUT}) of our hybrid complementary inverter varies from a high (5 V) to low (0 V) level as the input voltage (V_{IN}) varies from low (−2.5 V) to high (2.5 V) level, converting a logical 1 into a logical 0 and a logical 0 into a logical 1. These transfer characteristics of input–output voltage are deviated from the ideal operation of an inverter, which would have V_{IN} range of 0–5 V with a switching voltage ($V_{IN} = V_{OUT}$) at 2.5 V. To avoid this voltage-transfer characteristic (VTC) problem, an extra level-shifting element has been added in a circuit design,[18,30–32] but rendering it complicated and resulting in more power consumption.[31,32] For this reason, the inverter, showing desirable switching characteristics in the V_{IN} range from 0 to 5 V with a switching voltage at 2.5 V and a higher inverter gain was constructed by adjustment of the threshold-voltage position of the ZnO-nanowire FET with proton beam irradiation, as shown in the red filled symbols in Figure 3a and b. When the input voltage is 0 V (logical 0), the n-channel ZnO-nanowire transistor is OFF (p-channel SWNT-network FET is ON), setting the output voltage to 5 V (logical 1). When the input voltage is 5 V (logical 1), the p-channel SWNT-network FET is OFF, and the n-channel ZnO-nanowire FET is ON, inducing the output voltage to 0 V (logical 0). The logic inverter circuit of our hybrid nanodevices is simple in circuit configuration and presents less operating-power consumption with the absence of an additional level shifter.[30–32] Also, the VTC of our inverter circuit is nearly ideal due to high noise margin and high inverter gain with full swing characteristics and less static power dissipation than single-carrier type-based circuits.[32–34] Figure S4 in Supporting Information shows the statistical analysis of transition voltage and inverter gains for all fabricated hybrid complementary inverters with a supply voltage of

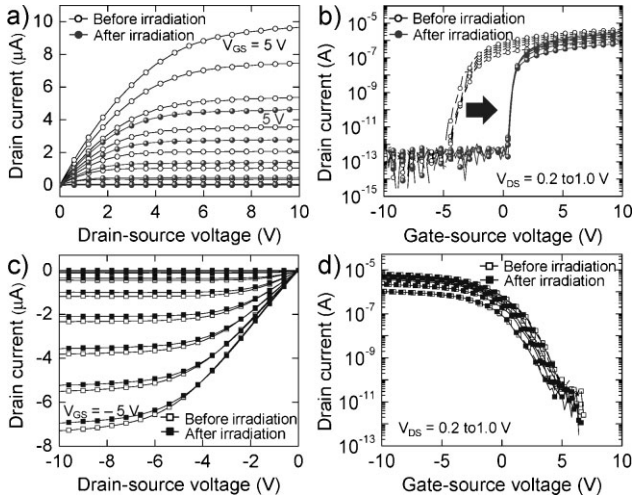

Figure 2. Characteristics of a ZnO-nanowire FET before (open circles) and after (filled circles) proton irradiation: a) I_{DS}–V_{DS} output characteristics for various V_{GS} from 1 to 5 V with a step of 1 V, and b) I_{DS}–V_{GS} transfer characteristics for various V_{DS} from 0.2 to 1 V with a step of 0.2 V. Characteristics of an SWNT-network FET before (open squares) and after (filled squares) proton irradiation: c) I_{DS}–V_{DS} output characteristics for various V_{GS} from 1 to −5 V with a step of −1 V, and d) I_{DS}–V_{GS} transfer characteristics for various V_{DS} from 0.2 to 1 V with a step of 0.2 V.

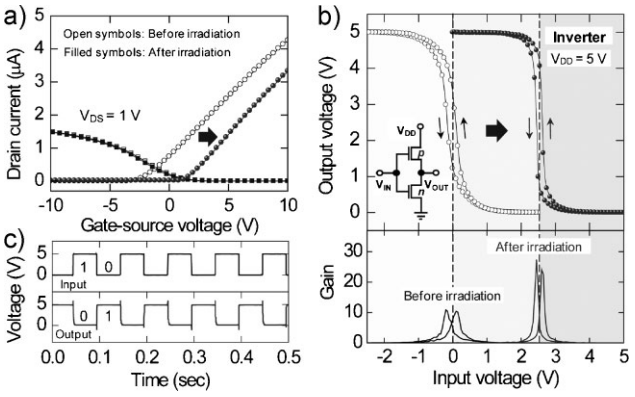

Figure 3. Characteristics for a hybrid complementary inverter. a) An overlay of I_{DS}–V_{GS} curves (at V_{DS} = 1 V) of the ZnO-nanowire and SWNT-network FETs before (open symbols) and after (filled circles and squares) proton irradiation, respectively. b) VTCs of a complementary inverter with changes in the switching voltage and inverter gain before (open symbols) and after (filled symbols) proton irradiation. The VTCs show output voltage and gain as a function of input voltage for supply voltage (V_{DD} = 5 V). The inset shows the circuit schematic of the inverter. c) Dynamic behavior of the inverter circuit. The upper curve shows the input waveforms and the lower curve shows corresponding output response of the inverter.

5 V before and after proton irradiation with a fluence of 1×10^{11} cm^{-2}.

In addition, the dynamic behavior of the inverter circuit after adjusting the switching voltage using a proton beam shows response to a square wave input signal (Fig. 3c). The dynamic transfer characteristics of the input–output voltage were clearly observed. We also carried out the experiment at a higher proton fluence of 1×10^{12} cm^{-2} with an energy of 10 MeV, (see Fig. S6 of the Supporting Information). The results exhibited a more positive shift to the threshold voltage of n-channel ZnO-nanowire FETs, due to more proton-radiation-induced electron trap charges generated at the ZnO/SiO_2 interface by a higher dose of proton. As a result, more trapping of the conduction electrons and the significant fraction of the surface depletion occurred in the nanowire channel. This causes a larger positive shift of the inverter transition region from high to low logic states. Therefore, it can suggest a method for selective adjustment of the logic operation of the specific hybrid inverter circuit for favorable switching characteristics through various proton-fluence conditions.

To implement basic computation based on the hybrid devices, we demonstrate other logic gates, such as NOR, NAND, and SRAM cells, using both p- and n-channel FETs connected in complementary configurations. Figure 4a shows the result for a NOR gate, which presents the output voltage as a function of the four possible input states (0,0), (1,0), (0,1), and (1,1). The circuit diagram for the NOR gate is shown in the inset of Figure 4a. When either one or both inputs (A and B) are a logical 1, at least one of the n-channel ZnO nanowires creates a conducting path, resulting in the output to be low (logical 0). The output is a logical 1 only when both inputs are a logical 0, because neither ZnO-nanowire FET is ON, while both p-channel SWNT-network FETs are ON. Figure 4b shows the result for a NAND gate. When both inputs are high (logical 1), the ZnO-nanowire channel in two series-connected n-type FETs become conducting between the output node and the ground, then the output voltage is low (logical 0). A high output voltage (logical 1) is achieved when either one or both inputs are a logical 0, that is, at least one of the parallel-connected p-channel SWNT-network FETs is turned on. In addition, a flip-flop memory element in the complementary-type SRAM cell was constructed,

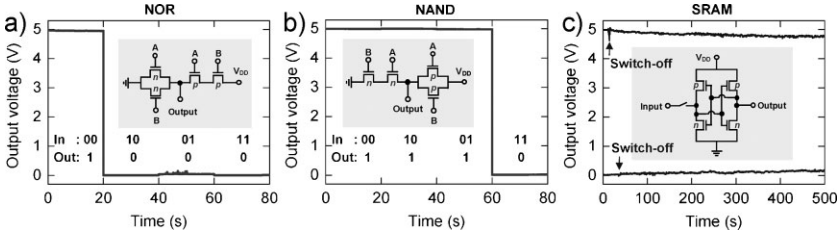

Figure 4. Hybrid complementary logic gates. a) Output voltage of a NOR gate as a function of the four possible input states: (0,0), (1,0), (0,1), and (1,1). The inset shows the circuit diagram of a complementary two-input NOR gate combining parallel-connected n-channel ZnO-nanowire FETs and series-connected p-channel SWNT-network FETs. b) Output voltage of a NAND gate as a function of the four possible input states: (0,0), (0,1), (1,0), and (1,1). The inset shows the circuit diagram combining two series-connected n-channel ZnO-nanowire FETs and the parallel-connected p-channel SWNT-network FETs. c) Output voltage of a flip-flop SRAM cell composed of cross-coupled hybrid complementary inverters. The inset shows the circuit diagram of the two-inverter bistable elements.

as shown in Figure 4c. The memory cell can preserve one of its two possible stable states (logical 0 or 1), through the set or reset input operation. To verify the operation of the memory cell, we set as a logical 1 state to the output by driving the input to 0 V. Then, the switch at the input was opened and it was observed the logical 1 state could be stored. Similarly, the memory cell maintained the logical 0 state by driving the input to 5 V followed by opening the input. Our complementary SRAM cell not only shows more stable storing time as compared to previous reports,[13] but also lower power dissipation and better noise immunity due to larger noise margins than, for example, the resistive-load SRAM cells.[33]

In summary, we presented a new layout of complementary logic circuit using p-channel SWNTs and n-channel ZnO-nanowire transistors. We showed that it was possible to achieve high-performance logic circuits by selectively controlling the threshold voltages of transistors through the population of proton-radiation-generated charges in the dielectric layer, and thus adjusting of logic level without additional compensation circuits, providing less power consumption and desirable switching characteristics. Using this approach, we demonstrated a complementary inverter, NOR and NAND logic gates, and a SRAM cell with an operation superior to devices and circuits based on a single carrier type and/or diodes. These results suggest that our hybrid approach is an attractive potential strategy toward more practical applications for digital integrated circuits with nanoscale materials and devices.

Experimental

Preparation of Purified SWNT Suspensions: A suspension of SWNTs obtained through an arc-discharge process (commercially available from Iljin Nanotech Co., Ltd., Korea) in 1,2-dichlorobenzene (o-DCB) (from Sigma–Aldrich) was prepared by a combination of sonication and centrifugation. In a typical experiment, 1 mg of SWNTs in 10 mL of o-DCB was sonicated for 5 min and the SWNT suspension was then centrifuged for 200 min at 16 000 × *g* followed by ultracentrifugation for 2 h at 325 000 × g. The upper 25% of the gray-transparent supernatant solution was then collected to prepare the highly individualized SWNT suspension.

Synthesis of ZnO Nanowires: ZnO nanowires were grown on Au-coated c-plane sapphire (c-Al_2O_3) substrates by thermally vaporizing a mixed source of commercial ZnO powder (99.995%) and graphite powder (99%) in a ratio of 1:1 in a horizontal tube furnace. A thin film of Au (~3 nm) was deposited on the c-plane sapphire substrate with an electron beam evaporator. The source materials and substrates were placed in an alumina boat and loaded at the center of the quartz tube. The ZnO nanowires were then grown on the substrates at a temperature of ~920 °C for 20–25 min under a flow of Ar (50 sccm) and O_2 (0.2 sccm).

Characterization Methodology for Proton Irradiation: Accelerated proton beams were generated using a MC-50 cyclotron (at the Korea Institute of Radiological and Medical Sciences, Seoul). The beam diameter was ~6 cm, its uniformity was ~90%, and the average beam current was 10 nA. In our study, the proton beam energy was 10 MeV and the total fluence of proton beam was 1×10^{11} or 1×10^{12} cm^{-2}, corresponding to a proton beam irradiation time of 600–6000 s, respectively.

Measurement of Electrical Properties: The current–VTCs of transistors and logic circuits were measured using a semiconductor parameter analyzer (Agilent B1500A). The evaluation of the AC electrical characteristics was performed using a pulse pattern generator (Agilent 81104A) and a digital oscilloscope (TDS 3054).

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