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Ultrathin Sticker-Type ZnO Thin Film Transistors Formed by Transfer Printing via Topological Confinement of Water-Soluble Sacrificial Polymer in Dimple Structure

Suk Ho Kim, Jongwon Yoon, Su Ok Yun, Youngkyu Hwang, Hun Soo Jang, and Heung Cho Ko*

To create ultrathin sticker-type electronic devices that can be attached to unconventional substrates, it is highly desirable to develop printable membrane-type electronics on a handling substrate and then transfer the printing to a target surface. A facile method is presented for high-efficiency transfer printing by controlling the interfacial adhesion between a handling substrate and an ultrathin substrate in a systematic manner under mild conditions. A water-soluble sacrificial polymer layer is employed on a dimpled handling substrate, which enables the topological confinement of the polymer residue inside and near the dimples during the etching and drying processes to reduce the interfacial adhesion gently, creating a high yield of transfer printing in a deterministic manner. As an example of an electronic device that was created using this method, a highly flexible sticker-type ZnO thin film transistor was successfully developed with a thickness of 13 μ m including a printable ultrathin substrate, which can be attached to various substrates, such as paper, plastic, and stickers.

1. Introduction

Membrane-type electronic devices based on organic and inorganic materials, including pentacene,^[1] rubrene,^[2] conducting polymers,^[3] carbon nanotubes,^[4] graphene,^[5] single-crystal silicon,^[6–8] GaN,^[9] InAs,^[10] GaAs,^[11] and ZnO,^[12] provide a lot of versatility to keep, handle, and use because the thin structure reduces weight and increases mechanical flexibility, thereby enabling deformation of their shapes. The fabrication of ultrathin devices is possible by using either direct wet/dry processes on a desired substrate or by fabrication of the materials on a different substrate, followed by transfer printing. In the latter case, it is highly desirable to control the interfacial adhesion between the donor substrate and the printable formats. The interfacial adhesion should be strong enough to provide

Dr. S. H. Kim, J. Yoon, S. O. Yun, Y. Hwang, H. S. Jang, Prof. H. C. Ko School of Materials Science and Engineering Gwangju Institute of Science and Technology (GIST) 1 Oryong-Dong, Buk-Gu, Gwangju 500-712, Korea E-mail: heungcho@gist.ac.kr



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a high degree of stability during fabrication but weak enough to enable transfer printing, as seen in examples such as laserinduced liftoff,^[13] heat-induced liftoff,^[14] and the use of a sacrificial layer.^[5–10,15,16] In particular, the transfer efficiency can be improved by using lateral/vertical inorganic anchors,^[17] peripheral polymer pedestals,^[18] geometrical confinements of concave/convex arrays,^[19] stamp-shaped designs,^[20] and the kinetic controls of printing speed and direction.^[20,21]

In relation to a substrate, if it is an ultrathin polymer film with a thickness on the order of tens of micrometers or less, high flexibility itself inevitably requires a supportive handling substrate and transfer printing of the final devices. Among the methods mentioned above, the use of a sacrificial layer seems to be the most useful because any material, including

SiO₂,^[6] metals,^[5,15] and polymers,^[8,16] can be used as a sacrificial material if the appropriate etchant exists. The use of a laser can damage the substrate, particularly polymeric substrates, and the use of heat also reduces the number of candidate materials according to their thermal expansion coefficients. However, when using a sacrificial layer, simple planar geometry can easily induce the removal of the ultrathin substrate from the handling substrate after complete etching. The use of anchors or pedestals in a selected area can somewhat tether the ultrathin substrate, but there is the risk of the ultrathin substrate not being fully free from partial suspension or wrinkle formation due to the irregular adhesion. This problem can be solved by using two-dimensional arrays of concavities on a handling substrate with SiO₂ as a sacrificial layer,^[19] but this solution requires a specific shape for geometrical confinement and HF etchant solution can be detrimental for certain materials, circuit designs, and fabrication processes due to its toxicity and poor selectivity.^[16]

In this paper, we suggest a facile method to control the interfacial adhesion in a systematic manner and to provide mild conditions for removing a sacrificial layer to avoid such hazardous and limited processes. We envisioned that a combination of a dimple array structure and a sacrificial polymer layer would enable the topological confinement of the polymer





Figure 1. a-f) Schematic illustration of the steps for fabricating printable ultrathin ZnO-based TFTs on a handling substrate and subsequent dry transfer printing.

residue near and inside the dimples, rather than in the planar region, during the etching and drying processes. The residue in the array would serve as a glue to uniformly tether the ultrathin layer. The sacrificial materials we chose in this study were water-soluble polyacrylic acid (PAA) and dextran due to their ability to be used under much milder conditions than those for SiO₂ or metals.^[16] We used spray- and spin-coating as our coating methods. We tested this idea by the transfer printing of ultrathin substrates with diverse lateral dimensions (ranging from 100 μm \times 100 μm for the smallest island to 3.0 cm \times 2.7 cm for the largest pattern) and diverse patterns (squares, circles, triangles, stars, numbers, ribbons, and meshes) on a rubber stamp. As an example of an electronic device that utilizes this method, we developed printable ZnO-based thin film transistors (TFTs) and carried out transfer printing on flexible substrates, namely a piece of paper and a PET film. We chose highly transparent ZnO as an active channel due to the easy access for the fabrication process at low temperature.^[22,23] A facile method of solution-based film formation without using metal-organic/plasma-enhanced/thermal chemical vapor deposition or sputtering offers the additional benefits of lowering fabrication costs and enabling processability on a flexible substrate in large area.^[23,24] In this study, we generated ultrathin TFTs with a thickness of \approx 13 µm that included a printable substrate and then manipulated them into stick-and-play forms on unconventional substrates.

2. Results and Discussion

Figure 1 depicts the fabrication procedure used to develop printable, ultrathin electronic devices. The procedure starts with the generation of dimple arrays on a handling substrate

by the patterning photoresist process using conventional photolithography, and the unprotected region is then recessed by reactive ion etching [RIE; $SF_6 = 40$ standard cubic centimeters per minute (sccm), 50 mTorr (where 1 torr \approx 133 Pa), 50 W] on a silicon wafer substrate (Figure 1a). Spray- or spin-coating polyacrylic acid (PAA) or dextran onto the substrate forms a sacrificial layer to facilitate transfer printing after the fabrication of the device (Figure 1b). Spin-coating SU-8 and curing the film generates an ultrathin substrate (Figure 1c). The polymer inside the dimples replicates the shapes during the curing process. The fabrication of ultrathin electronic devices, such as ZnObased TFT arrays, on the top of the substrate can then be initiated through the conventional fabrication methods of growing, depositing, and etching (Figure 1d). After the device fabrication process has been completed, the sacrificial layer is removed in water, which partially suspends the planar region except for the dimples, with maintenance of the lateral position of the devices (Figure 1e). The ultrathin device can be retrieved through van der Waals adhesion forces by placing a polydimethylsiloxane (PDMS) slab in contact with the surface of the device and peeling the PDMS stamp back (Figure 1f).^[25] The transferred device can be reprinted on various target substrates, such as a plastic film, a piece of paper, and a sticker, using a glue layer (Figure 1g). The handling substrate is reusable after a simple cleaning process in a piranha solution.

Figure 2a shows dimple arrays (pitch = 20 μ m, cross shape, depth = 3.9 μ m) on a silicon wafer generated by RIE (SF₆ = 40 sccm, 50 mTorr, 50 W, 7 min). With regard to the generation of the sacrificial layer, the selection of a proper material, a proper deposition method, and appropriate etching conditions is very important not only for providing stability in the fabrication of the device but also for protecting the inner parts of the device during the etching of the layer. In the case of a SiO₂ layer, the

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Figure 2. a-c) SEM images, in both tilted and cross-sectional views of the samples to generate a layer of printable ultrathin substrate on a silicon handling substrate: a) after generating dimple arrays on a silicon wafer chip, b) after spray-coating a water-soluble dextran layer, and c) after patterning a SU-8 substrate onto the handling substrate. d) Cross-sectional SEM images of the sample in (c) before and after etching in water for 30 min. e) Photograph of a printable ultrathin SU-8 substrate on a silicon chip after etching the sacrificial layer. f) Photograph and SEM images of the SU-8 pattern printed on a PDMS slab.

strong acid (HF) aqueous etching solution penetrates through SU-8 or the polyimide layer to attack the inner layer; the damage to the inner Al layer encapsulated by SU-8 (thickness: 1.5 µm) or PI (thickness: 1.2 µm) resulting from the dropping of a droplet of HF solution on the top of the polymer surface for 5 min can be seen in the Supporting Information. On the other hand, PAA and dextran require water as an etchant, which, in contrast to HF, does not attack the inner Al layer. Spray-coating the polymer solution on the handing substrate generates a sacrificial layer with multiform thicknesses, as shown in Figure 2b. The temperature of the substrate was maintained at 150 °C to rapidly dry the droplets and maintain the uneven topology of the polymer layer. At low temperatures, adjacent droplets will merge together to form a relatively more uniform thickness. The amount of the sacrificial layer was controlled by varying the spray time of the polymer solutions. Spray-coating preserves the dimple structure and enables a large area to be coated more efficiently compared with spin-coating or free-standing coating. This result is due to the statistical effect of covering the same amount of a material with a two-dimensional unit area regardless of the surface topology (see the Supporting Information).^[26] Continuous spray-coating enables conformal coverage on both the planar and recess regions when the amount of spray-coated dextran or PAA reaches 0.109 or 0.051 mg/cm², respectively (see the Supporting Information). Figure 2c shows 12-µm-thick SU-8, with lateral dimensions of 500 μ m \times 500 μ m, which fills the dimples inside the pattern. The sacrificial layer was not etched during the SU-8 patterning process. The patterning process using RIE after finishing a device also makes it possible to prevent the sacrificial layer from being etched during the device fabrication. Dipping the sample in water at 50 °C

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etched the sacrificial layer, with the exception of some residue inside and near the dimples (Figure 2d); a longer etching time reduces the amount of the sacrificial residue (see the Supporting Information). Figure 2e shows the printable SU-8 layer on a silicon chip with maintenance of the position of the pattern after dipping the sample in water for 30 min. Because the polymer residue serves as glue used to tether the ultrathin SU-8 pattern to the handling substrate, the adhesion was not dramatically reduced but was instead reduced gently to achieve both the maintenance of the position and a high yield of transfer printing, even after the water reached the center of the pattern. Placing a PDMS slab on the donor substrate and picking it up results in the retrieval of the SU-8 laver together with pimples (Figure 2f). The polymer residues remained on the printed ultrathin substrate and the handling substrate after transfer printing can be removed by washing with water (see the Supporting Information).

Because the amount of the topologically confined sacrificial layer should affect the efficiency of transfer printing, we examined the alignment degree (AD; the number of ultrathin substrate islands that maintain

their position on a handling substrate after removing the sacrificial layer divided by the total number of the initial islands) and transfer yield (TY; the number of ultrathin substrate islands transferred to a target substrate divided by the total number of printable islands before transfer printing) of a SU-8 pattern (18 \times 18 square island arrays, lateral dimension = 500 μ m \times 500 μ m, thickness = 12 μ m) as a function of etching time in water at 50 °C (Figure 3a). Naturally, shorter etching times (e.g., less than 15 min) result in an AD of 100% but a TY of less than 100% due to the presence of a large amount of sacrificial polymer residue. A sufficient etching time (e.g., 30 min or more) provides an AD and a TY of 100%; this value was even maintained following much longer etching times (e.g., 10 h). On the other hand, with no dimple structure on the handling substrate, we could not achieve both an AD and a TY of 100%. We also confirmed this behavior by measuring the interfacial adhesion force between the ultrathin SU-8 substrate and a handling substrate (Figure 3b and Supporting Information). To ensure the attainment of significant values of the adhesion force with our equipment and experimental setup, we used a single square pattern of SU-8 with lateral dimensions of 5 mm \times 5 mm. We note that a much longer etching time is required in this test to achieve a TY of 100% than in the case corresponding to Figure 3a. In the case where dimples were formed, after an insufficient etching time (i.e., up to 420 min), we observed strong adhesion forces above 1 N, with the partial transfer of SU-8 in only a specific area (see zone A of Figure 3b). A sufficient etching time decreases the adhesion force to $\approx 0.5-1$ N to yield values of 100% for both AD and TY (zone B). Of course, an excessive etching time reduced the adhesion force to below 0.5 N and did not guarantee a perfect AD (zone C). On the other hand, in the



Figure 3. a) Alignment degree (AD) and transfer yield (TY) of 18 × 18 SU-8 square island arrays (lateral dimensions = 500 μ m × 500 μ m, thickness = 12 μ m). b) Adhesion force of a SU-8 square pattern (lateral dimensions = 5 mm × 5 mm, thickness = 12 μ m) as a function of etching time. Insets of (a) and (b): photographs of the samples after etching the sacrificial layer in water for 30 min (a) and 10 h (b).



case where no dimple was formed, we were unable to find zone B with moderate adhesion forces due to the absence of the tethering effect.

We also investigated the influence of the amount of PAA and dextran added by spray-coating and spin-coating on the AD and TY (Figure 4a,b). In the case of spray-coating, the amount of the deposited sacrificial layer on a handling substrate was controlled by altering the spray time (see the Supporting Information). Spray-coating relatively smaller amounts of the sacrificial layer (i.e., 0.08 mg/cm² of dextran or less) does not cover the handling substrate, so direct contact between the two substrates occurs in the bare surface area, resulting in a low TY with some torn patterns due to the strong adhesion in the region (see the Supporting Information). On the other hand, an excessive amount of coating (i.e., 0.2 mg/cm² of dextran) covers the entire area and even fills the coverture of the dimples, causing the loss of the topological confining effect and thereby easily dislocating the position of the ultrathin substrate after the removal of the sacrificial layer. As a result, the optimum amounts of spray-coated dextran and PAA to ensure AD and TY values of 100% were 0.109 to 0.134 mg/cm² (corresponding spraying time: ≈9-11 s) and 0.051 to 0.063 mg/cm² (≈10-12 s), respectively. In the case of spin-coating, the thickness of the sacrificial layer was controlled by coating the polymers at different concentrations at the same spin speed of 2000 rpm (see the Supporting Information). There is an appropriate concentration range to ensure complete coverage of the area without filling the dimples significantly; too low of a concentration did not cover the entire area due to a dewetting phenomenon, whereas too high a concentration completely covered the area but significantly filled the dimples (see the Supporting Information). The optimal amount of spin-coated dextran and PAA to ensure AD and TY values of 100% were 0.302 to 0.414 mg/cm²



Figure 4. a,b) AD and TY of 18×18 SU-8 square islands (lateral dimensions = 500 μ m × 500 μ m, thickness = 12 μ m) as a function of the amount of dextran and PAA deposited by a) spray-coating and b) spin-coating on handling substrates with cross-shaped dimples.

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Figure 5. a–c) Photographs and OM images of various patterns of ultrathin SU-8 films on PDMS slabs after transfer printing. A Cr layer (thickness = 100 nm) was additionally deposited prior to transfer printing to achieve better contrast.

(corresponding concentration range: \approx 10–14 wt%) and 0.193 to 0.207 mg/cm² (\approx 6–7 wt%), respectively.

Under optimized conditions, we successfully transferred diverse patterns of a SU-8 layer, including squares (side

= 100–500 µm), circles (diameter = 100–500 µm), triangles (side = 100–500 µm), stars (side = 36–290 µm), numbers (size = 300 µm × 500 µm), ribbons (width = 150 µm, length = 2.4–5 mm), and a mesh (overall dimensions = 1.8 mm × 4.8 mm, size of each island = 300 µm × 300 µm, size of each interconnect = 100 µm × 400 µm), to a PDMS slab (**Figure 5a**). Uneven optical contrast of the transferred patterns in OM images reflects the multiform thicknesses of the spray-coated sacrificial layer. Printing the SU-8 layer in a large area (size of square = 9 mm × 9 mm, size of a cartoon dog = 3.5 cm × 2.5 cm) is also possible (Figure 5b,c). We note that larger patterns require longer etching times if there is no hole inside the pattern; for example, an etching time of 15 h was required for the cartoon dog.

To demonstrate the process of first fabricating a device and then performing transfer printing for a stick-and-play system, we prepared a printable ultrathin ZnO TFT array on a silicon wafer (**Figure 6**a). Each TFT consists of a gate electrode (Al, thickness = 100 nm), a gate dielectric layer (c-PVP, thickness = 200 nm), a channel layer (ZnO, thickness = 80 nm), and source/ drain electrodes (Al, thickness = 100 nm) on the ultrathin substrate (SU-8, thickness = 12 μ m). Double transfer printing using a PDMS stamp enables indirect device formation on unconventional substrates. When using a PDMS slab for the first transfer printing and a photo-curable glue layer and a piece of paper for the second transfer printing (Figure 6b), the TY was 100%



Figure 6. a) Photograph (left) and SEM images in tilted view (middle) and cross-sectional view (right) of printable ZnO TFTs on a silicon wafer chip. b) ZnO TFTs transferred to a piece of paper coated with photo-curable NOA. c) ZnO TFTs on a sticker that are temporarily attached to a non-stick piece of paper. d) ZnO TFTs on a sticker from the sample in (c)that are attached to a pen. e) $I_{DS}-V_{GS}$ and (f) $I_{DS}-V_{DS}$ characteristics of a representative TFT on the sample in (b).



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www.MaterialsViews.con (a) (b) r (mm) 10 42 5.1 10 .71 ∞ 7.9 5.1 43 10⁻¹⁰ 5 mm 10 -10 20 V_{GS} (V) (C) (d) 10⁶ 10⁵ - V^S (V) 2 2 10 μ/μ₀, <mark>V</mark>₇ . O 10³ ۰°۲η/۲ 10 Compressive Tensile Tensile @ r = 4.3 mm -2 10² 10⁰ -4.2 -5.1 -7.1 × 7.9 5.1 4.3 10² 10³ **10**⁴ 10⁰ 10¹ Bending Radii (mm) Bending cycles

Figure 7. a) Photograph of ZnO TFTs transferred to a PET film. b) $I_{DS}-V_{GS}$ characteristics of the ZnO TFT as a function of bending radius; inset: photograph of a bending stage with the sample. c,d) Relative mobility (μ/μ_0), threshold voltage difference ($V_T-V_T^{\infty}$), and on/off current ratio (I_{on}/I_{off}) of the device as a function of bending radius (c) and bending cycles between bending radii of ∞ to 4.3 mm in tensile mode (d).

(total of 48 TFTs), with negligible distortion of the pitch of the arrays (within 2.7%) (see the Supporting Information). Temporarily keeping the devices on a sticker (Figure 6c) and attaching them later to various surfaces, including the round surface of a pan, a piece of paper, a cellular phone, and the skin of a hand, constitutes another stick-and-play system (Figure 6d and Supporting Information). When the device is directly transferred to a sticker without using a PDMS stamp, the TY was 100%, with distortion within 1.3% (see the Supporting Information).

To determine the electronic performance of the transferred ZnO TFTs, we examined a randomly chosen representative TFT that was on a piece of paper (Figure 6b). It showed typical n-type behavior with a saturation mobility of 0.11 cm² V⁻¹ s⁻¹, which is similar to those of ZnO-based TFTs directly fabricated on a relatively thick PET film or a polyacrylate film (thickness: 200 μ m) through solution process by other groups (Figure 6e,f).^[27] The on/off current ratio of 10⁴ at a V_{DS} of 15 V is one to two orders of magnitude larger than that of the ZnO TFTs directly fabricated on plastic substrates; this result presumably arises from the local gate configuration of our device and the stable fabrication process that is achieved using a rigid handling substrate. The positive threshold voltage (5.6 V) enables enhancement mode in TFT operation, which is more preferable for simplification of circuits and minimization of power dissipation.^[28]

We also investigated the electronic performance of ultrathin ZnO TFTs as a function of the bending radius by transferring samples to a polyethylene terephthalate (PET) film (**Figure 7**a), which provides more stable conditions for handling and probing the sample. The average saturation mobility, threshold voltage, and on/off current ratio for 10 different, planar-shaped TFTs

were 0.09 \pm 0.025 cm² V⁻¹ s⁻¹, 5.4 \pm 0.6 V, and (1 \pm 0.72) \times 10⁵, respectively (see the Supporting Information). We examined the flexibility of the device by measuring the transfer curve of the device upon modulation of the bending radius stepwise from -4.2 mm (compressive mode of the TFTs) to 4.3 mm (tensile mode) (Figure 7b) and upon bending cycles up to 10 000 between bending radii of ∞ to 4.3 mm in tensile mode (Supporting Information). The electronic performance of the device is very stable, with no considerable difference in the three parameters upon the bending radii and cycles; the relative mobility was less than 22%, the threshold voltage shift was between -0.7 and 0.35 V, and the on/off ratio was above 10^4 (Figure 7c,d). In particular, it should be noted that trapping effect and/or damage caused by oxygen and moisture under the ambient conditions in the gate dielectric layer during measurement may also involve the change in the electronic performance (see the Supporting Information).^[29]

3. Conclusions

This paper suggests an advanced methodology to manipulate an ultrathin device into printable formats on a handling substrate. Employing a water-soluble sacrificial polymer layer on a handling substrate with dimple arrays provides not only mild conditions for etching but a platform to develop printable membrane-type electronic devices. Topological confinement of the polymer residue located inside and near the dimples enables the gradual reduction of the interfacial adhesion between a handling substrate and an ultrathin polymer substrate to



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achieve a high yield of transfer printing in a deterministic manner. Transfer-printing using diverse shapes of the ultrathin substrate on various substrates, such as paper, plastic, and tape, with 100% AD and TY is achieved under optimized conditions. The provided example of transfer printing using highly flexible membrane-type ZnO TFTs demonstrates the possibility for developing sticker-type electronic devices.

Experimental Section

Preparation of an Ultrathin Substrate on a Handling Substrate: All silicon wafer chips (Prolog Semicor, Ltd., 100) used as handling substrates were cleaned with acetone, IPA, and deionized water (Millipore, resistance: \approx 18 MΩ) and then dried at 110 °C for 1 min immediately prior to use. The PR masking layer on a handling substrate was prepared by spincoating an adhesion promoter (HMDS, AZ AD promoter-K, 3500 rpm, 35 s), a PR layer (AZ 1512, 3500 rpm, 35 s, followed by soft baking at 110 °C for 90 s) and patterning array of cross-type holes (pitch: 20 µm) through contact-mode lithography using a mask aligner (CA-6M, SHINU MST, illumination: 8.5 mW/cm², 15 s) and an aqueous developer (MIF 500, 40 s). Reactive ion etching (RIE; 50 mTorr, 40 sccm SF₆, 50 W, 7 min) and cleaning in acetone, a piranha solution $(H_2SO_4:H_2O_2 =$ 3:1 for 5 min), and deionized water generated dimple structures on the silicon chip. Spraying dextran (molecular weight = 70 000 g/mol, 2 wt%) or PAA (molecular weight of PAA = 50 000 g/mol, 2 wt% PAA solution was neutralized by NaOH prior to use) aqueous solutions on the dimple substrate using an airbrush (DB air brush, Nozzle diameter: 0.3 mm) at a deposition rate of 0.6 mg $cm^{-2} min^{-1}$ (height of nozzle = 28 cm, N_2 pressure = 0.2 MPa) generated a water-soluble sacrificial layer (see the Supporting Information). The temperature of all of the handling substrates was kept at 150 °C for the spray-coating and drying processes. Next, spin-coating SU-8 2010 (MICRO CHEM, 500 rpm for 5 s, 3000 rpm for 10 s), soft-baking them at 140 °C for 1 min, illuminating them with UV light (CA-6M, illumination: 8.5 mW/cm², 5 s), post-baking them at 95 °C for 2 min, and developing them in a SU-8 developer (50 s) provided an ultrathin substrate pattern with a thickness of $\approx 12 \ \mu m$.

Measurement of Adhesion Force: The adhesion force between the SU-8 pattern and the handling substrate was measured using a digital force gauge (DS2-5N, IMADA Co, Ltd.) and a motorized linear actuator (LTS-HS, Newport). Both surfaces of the digital force gauge planar tip (radius = 13 mm) and SU-8 pattern (lateral dimensions = 5 mm \times 5 mm, thickness = 12 μ m) were attached by double-stick tape (3M, lateral dimensions on pattern = 5 mm \times 5 mm) prior to testing. The gauge was depressed onto the SU-8 pattern and pulled up slowly at a rate of 0.1 mm/s.

Fabrication of Printable ZnO TFTs: A pattern of the ultrathin SU-8 substrate (thickness: 12 μ m) was prepared on a Si handling wafer substrate by the method mentioned previously. On the patterned SU-8 film, Al (thickness: 100 nm) was deposited through a shadow mask by an e-beam evaporator (Korea Vacuum Tech., Ltd.) to form a gate electrode. Spin-coating crosslinkable poly(4-vinylphenol) (c-PVP) solution at 3000 rpm for 35 s and performing annealing at 200 °C for 1 h forms a gate dielectric layer (thickness: 200 nm and $\varepsilon_r = 3.6$).^[30] The c-PVP solution was prepared by dissolving 5 wt% PVP powder and 5 wt% poly(melamine-co-formaldehyde) methylated in propylene glycol monomethyl ether acetate (PGMEA). Next, the water-soluble sacrificial layer was etched at 50 °C in water for approximately 1 h prior to the formation of a semiconductive layer. ZnO (thickness: 80 nm), as an active layer, was deposited on the gate dielectric layer by spin-coating a ZnO solution, prepared by a method in the literature,^[31] at 3000 rpm for 35 s and annealing it at 200 $^\circ C$ for 2 h. Finally, Al (thickness: 100 nm) was deposited by an e-beam evaporator through a shadow mask to generate source and drain electrodes.

Transfer Printing: PDMS stamps were prepared by mixing and curing Sylgard 184 silicone elastomer base and Sylgard 184 silicone elastomer curing agent (10:1 by weight) at 70 °C for 2 h. After etching the sacrificial layer by dipping the samples in deionized water for at least 30 min, a PDMS slab was brought into contact with the ZnO TFT arrays and peeled back, transferring the arrays to the stamp. To reprint the arrays from the elastic stamp onto a piece of paper, a photocurable adhesive (NORLAND OPTICAL ADHESIVE 61, NORLAND PRODUCTS, INC.) was added at the interface between the two substrates and cured via UV light for 1 min. In the case of transfer printing onto an adhesive PET film, no additional adhesive layer was used. Next, peeling the target substrate off the PDMS completes the transfer printing. When a sticker is used instead of a PDMS stamp, the TFTs can be transferred to a sticker by placing the tape on the donor substrate and peeling it off.

Device Characterization: The measurement of current–voltage (I-V) for the fabricated devices was carried out using a semiconductor device analyzer (Agilent B1500A). SEM images were obtained using a Hitachi S-4700 microscope after depositing platinum (thickness: 7 nm) onto the samples.

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