DOI: 10.1002/adma.200800691

Piezoelectric Effect on the Electronic Transport Characteristics of ZnO Nanowire Field-Effect Transistors on Bent Flexible Substrates**

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The demand for flexible electronic components is increasing in portable handheld displays and communication products due to their light weight, flexibility, shock resistance, and low cost transparency.[1] Flexible electronics on plastic substrates have been approached quantitatively utilizing amorphous silicon, organic semiconductor materials, carbon nanotubes, and nanowires.[2] Among these, amorphous silicon plays an important role as an active matrix for optoelectronic devices through vacuum deposition techniques, but is limited by low mobility that restricts its application in high performance devices.[3] An alternative approach is the use of organic semiconductor materials. The merits of this approach include that it is a solution-based, room-temperature process, and that it involves low fabrication costs,[4] but low mobility is still an issue to overcome in this field.[5] On the other hand, inorganic nanowires have shown potential for various functional materials and devices due to their novel semiconductor properties such as the quantum confinement effect, less scattering of the carrier, and higher mobility exceeding their bulk counterpart.[6] Additionally, the flexibility of the nanowires enables them to be used in plastic electronics applications. Many efforts have been made to fabricate nanowire electronic devices, such as nanowire field-effect transistors (FETs) on plastic substrates.[2d,7] For example, Duan et al. have demonstrated the fabrication of high-performance thin film transistors on plastic substrates by using Si nanowires or CdS nanoribbons with a fluidic alignment method.[8] Other approaches employing GaAs or Si nanowires have been used for flexible nanowire FETs on plastic substrates.[9] However, relatively less effort has been devoted to understanding the electrical characteristics of nanowire flexible devices when nanowires are bent together with plastic substrates. It will be important to investigate the operational characteristics of bent nanowire flexible FETs for future applications in plastic electronics.

In particular, ZnO nanowires have received great interest among 1D-nanostructures, such as semiconducting nanowires, nanobelts, and carbon nanotubes, due to their multi-functionality. This multi-functionality also suggests their potential use in various applications such as sensors, FETs, displays, solar cells, and nanoscale generators.[10–14] Additionally, ZnO is well known as a piezoelectric material. Recently, a few studies have been done on the piezoelectricity of quasi-1D ZnO nanostructures of nanowires and nanobelts.[15] For example, Wang et al. have reported that the electrical characteristics of a ZnO nanowire are changed by bending the ZnO nanowire attached on a tungsten needle tip in a scanning electron microscope (SEM) chamber due to its piezoelectric property.[16]

We demonstrate the electrical characteristics of ZnO nanowire FETs fabricated on poly(ethylene terephthalate) (PET) substrates with a polymer gate dielectric. The transistor properties of ZnO nanowire FETs on flexible substrates are influenced when the substrates and nanowires are bent under various radii of curvature. This bending effect of the ZnO nanowire FETs is different between bottom-gate and top-gate FET device structures where the gate electrode is located under the nanowire or on top of the nanowire, respectively (Fig. 1). The different electrical characteristics of the different device structures can be explained by the piezoelectric effect and the electron trapping at the interfaces between the ZnO nanowire and the polymer dielectric.

Our device fabrication began with the growth of ZnO nanowires through the vapor–liquid–solid method mediated with Au catalysts on *c*-plane sapphire substrates. The field-emission scanning electron microscopy (FESEM) image in Figure 1a shows ZnO nanowires that were grown vertically. The insets of Figure 1a display a high-resolution transmission electron microscopy (HRTEM) image and a selected area electron diffraction (SAED) pattern, indicating that ZnO nanowires are single crystalline and have a (0001) growth direction. The details of the growth and the characterization of ZnO nanowires have been published elsewhere.[17]

To investigate the bending effects of ZnO nanowire flexible FETs, we fabricated two different FET device structures: bottom-gate and top-gate FET structures on PET substrates (Fig. 1c). These two device structures are distinguished by the

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[**] This work was supported through the Proton Accelerator User Program of the Ministry of Science and Technology of Korea, the National Research Laboratory (NRL) Program of the Korea Science and Engineering Foundation (KOSEF), the Program for Integrated Molecular Systems at GIST, and the SystemIC2010 project of the Korean Ministry of Commerce, Industry and Energy.

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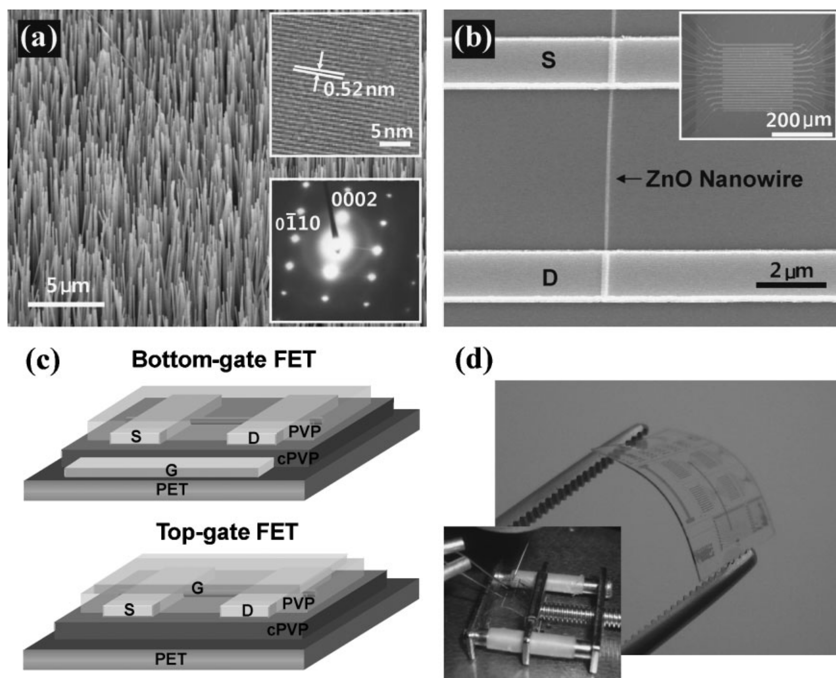

Figure 1. a) FESEM image of single crystalline ZnO nanowires grown on an Au-coated *c*-plane sapphire substrate. The insets show a HRTEM image (top) and corresponding SAED pattern (bottom). b) SEM image of a device where a ZnO nanowire is connected across the source (S) and drain (D) electrodes in a bottom-gate FET device. The inset is a SEM image showing the overall device area. c) Schematics of bottom-gate and top-gate FET device structures. d) Optical pictures show a demonstration of the bending of ZnO nanowire FET devices with a tweezer (right), and the measurement setup (lower left) characterizing ZnO nanowire FETs on the plastic substrate while the substrate and nanowires are bent.

location of the gate electrode relative to the nanowire. A 50 nm thick layer of Au was deposited for the bottom-gate or top-gate gate electrodes, and Ti/Au was deposited for the source (S) and drain (D) electrodes to provide the ohmic contact with the ZnO nanowire. Figure 1b shows a FESEM image of a single ZnO nanowire connecting across the source and drain electrodes in the bottom-gate FET device structure. As schematically illustrated in Figure 1c, the polymer dielectric layer was used for both types of FETs. Compared with inorganic dielectric materials, polymer dielectrics attract great interest for such merits as being low cost and having an easy fabrication process via spin-coating at room temperature. Therefore, an expensive vacuum system is not needed for the fabrication of the polymer dielectric layer. In our study, cross-linked poly(4-vinylphenol) (PVP) was used as a bottom-gate dielectric, and a top-gate dielectric was prepared by PVP in an isopropyl alcohol (IPA) solvent. A demonstration of the flexibility of nanowire FETs on a PET substrate and a picture of the measurement setup for electrically probing the ZnO nanowire flexible FETs are shown in Figure 1d.

The electrical characteristics of ZnO nanowire FETs on flexible PET substrates when the nanowires and substrates were not bent are summarized in Figure 2. Figures 2a and c show the representative data of the source–drain current versus voltage (I_{DS}–V_{DS}) characteristics measured at different gate biases for bottom-gate and top-gate nanowire FETs, respectively. Figures 2b and d display the source–drain current versus gate voltage (I_{DS}–V_G) measured at a fixed source–drain voltage of 0.1 V for the bottom-gate and top-gate nanowire FETs, respectively. The carrier concentration (at $V_G = 5$ V) was estimated as $\sim 1.9 \times 10^{17}$ and $\sim 1.8 \times 10^{17}$ cm^{-3}, and the mobility was estimated as $\sim$170 and $\sim$69 cm^2 V^{-1} s^{-1} for the bottom-gate and top-gate FETs, respectively. Both types of FETs exhibited typical n-type semiconductor characteristics, which are due to the presence of intrinsic donor-type defects induced by deviations from stoichiometry between Zn and O components during the synthesis of the nanowires.[18] The linear I_{DS}–V_{DS} curves at low bias suggest that the Ti electrodes have good ohmic contact with ZnO nanowires in both types of FETs. Note that the transistor characteristics of the ZnO nanowire flexible FETs with the polymer gate dielectric are comparable to the ZnO nanowire FETs on conventional SiO_2/Si substrates (data not presented here).

Figure 3 shows the representative electrical characteristics of the bottom-gate and top-gate ZnO nanowire FETs when they were bent with different bending radii using the measurement setup shown in Figure 1d. Figures 3a and c show a series of I_{DS}–V_G curves for different bending configurations, measured at a source–drain voltage of 0.1 V for bottom-gate and top-gate nanowire FETs, respectively. A smaller bending radius means increased bending, as schematically illustrated in the inset of Figure 3b. The strain

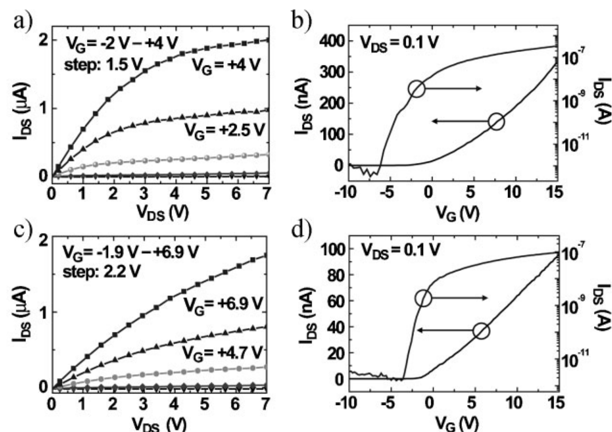

Figure 2. I_{DS}–V_{DS} characteristics (a and c) measured at different gate biases, and I_{DS}–V_G characteristics (b and d) measured at a fixed source–drain voltage of 0.1 V for a bottom-gate ZnO nanowire FET (a and b) and top-gate ZnO nanowire FET (c and d) while the ZnO nanowires were not bent.

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values described in the top horizontal axes in Figure 3b and d were calculated using an equation reported as[19]

$$Strain = \frac{t_{PET} + 2r}{2R_C} \times 100 \quad (1)$$

where r is the nanowire radius, t_{PET} is the thickness of PET substrate (~200 μm), and R_C corresponds to the radius of the curvature of bending. The nanowire radius of each device was measured by an atomic force microscope (AFM) after the electrical characterization of the devices. As the nanowire FETs were bent more, the source–drain current increased for a given gate bias and the threshold voltage (V_T) shifted to the negative gate bias direction for the bottom-gate ZnO nanowire FET, whereas the current decreased and V_T shifted to the positive gate bias direction for the top-gate ZnO nanowire FET. The shift of V_T is summarized as a function of bending radius and strain in Figure 3b and d for bottom-gate and top-gate nanowire FETs, respectively. These opposite trends of current change and V_T shift in the bottom-gate and top-gate ZnO nanowire FETs with bending are due to the piezoelectric effect of ZnO materials with an interface effect, which is explained later in detail.

The threshold voltages can be used to estimate the carrier concentration from the total charge, $Q_{tot} = C_g|V_g - V_T|$ in the nanowire, where C_g is the gate capacitance and V_T is the threshold voltage required to deplete the nanowire.[17] The gate capacitance can be estimated using a model of a cylinder on an infinite metal Plate [17,20]

$$\frac{C_g}{L} = \frac{2\pi\varepsilon_r\varepsilon_0}{\cosh^{-1}\left(\frac{r+h}{r}\right)} \quad (2)$$

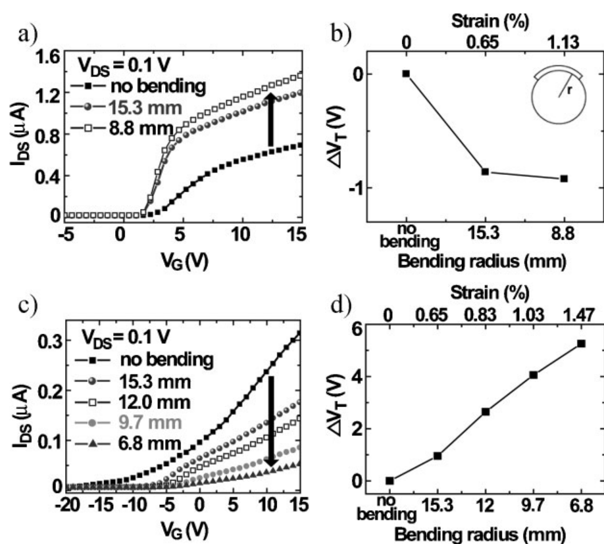

Figure 3. I_{DS}–V_G characteristics (a and c) and threshold voltage shift (ΔV_T) (b and d) at various radii of curvature for a bottom-gate ZnO nanowire FET (a and b) and a top-gate ZnO nanowire FET (c and d). The inset in (b) shows a schematic for bending radius.

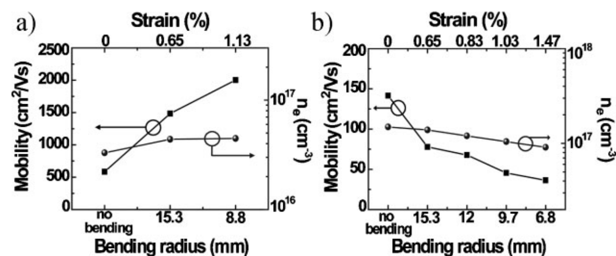

Figure 4. Mobility and carrier concentration as a function of bending radius and strain for a bottom-gate ZnO nanowire FET (a) and a top-gate ZnO nanowire FET (b). The mobility was estimated where the g_m is maximum, and the carrier concentration was determined at $V_G = 5$ V.

where r is the nanowire radius, L is the nanowire channel length (~4 μm), h is the polymer dielectric layer thickness, ε_0 is the permittivity of free space, and ε_r is the dielectric constant of PVP ($\varepsilon_r = 3.9$)[21] or cross-linked PVP ($\varepsilon_r = 3.6$).[22] The thicknesses of the PVP dielectric layers were 200 nm and 900 nm for the bottom-gate and top-gate FETs, respectively, as measured by AFM. The carrier concentration, $n_e = Q_{tot}/e\pi r^2 L$, can be determined at a gate bias of 5 V and is summarized in Figure 4. Before bending, the carrier concentrations of bottom-gate and top-gate FETs were 3.3×10^{16} and 1.4×10^{17} cm^{-3}, respectively. With more bending, the carrier concentration of the bottom-gate ZnO nanowire FET increased from 3.3×10^{16} (no bending) to 4.5×10^{16} cm^{-3} (at 1.13% strain, 8.8 mm bending radius) (Fig. 4a), whereas that of the top-gate ZnO nanowire FET decreased from 1.4×10^{17} (no bending) to 1.0×10^{17} cm^{-3} (at 1.47% strain, 6.8 mm bending radius) (Fig. 4b). The carrier mobility values, μ_e, for the ZnO nanowire FETs can also be calculated using Equation 3 and are plotted in Figure 4.

$$\mu_e = \frac{dI_{DS}}{dV_G}\frac{L^2}{V_{DS}C_g} \quad (3)$$

The estimated mobility values for the bottom-gate ZnO nanowire FET increased (Fig. 4a) with more bending, whereas those for the top-gate ZnO nanowire FET decreased (Fig. 4b). Assuming that the effective channel width (W) equals the nanowire diameter, the estimated normalized transconductance (g_m/W, where $g_m = dI_{DS}/dV_G$)[23] increased from 0.95 μS μm^{-1} (no bending) to 3.26 μS μm^{-1} (1.13% strain, 8.8 mm bending radius) for the bottom-gate FET, whereas it decreased from 180 nS μm^{-1} (no bending) to 40 nS μm^{-1} (1.47% strain, 6.8 mm bending radius) for the top-gate FET. Therefore, the mobility change is mainly due to the variations of the transconductance with bending of the FETs. The transconductance is directly related to the efficiency of gating on the channel of the nanowire FET and the trapping of electrons at the interface between the nanowire and polymer dielectric,[24] which affects the carrier density inside the conducting channel of nanowire. The increase of transconductance in the bottom-gate FET demonstrates that the trapping

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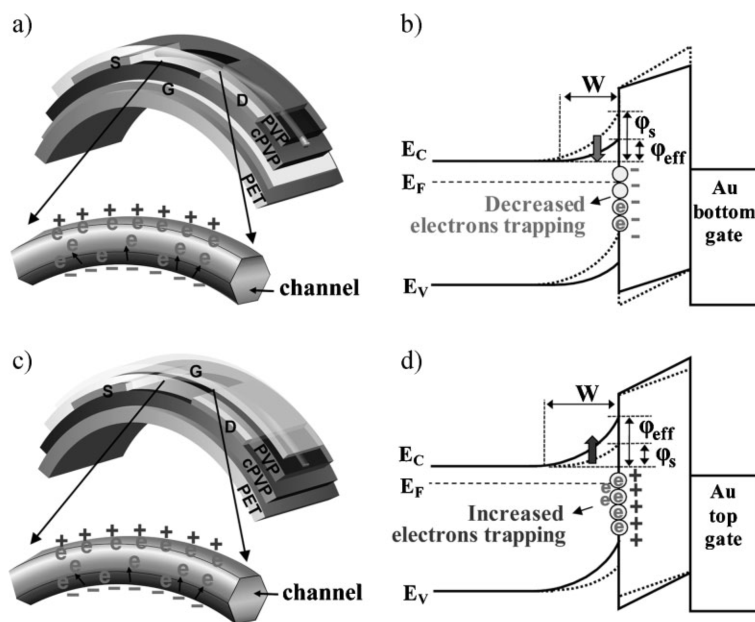

Figure 5. Schematic diagrams illustrating the piezoelectric effect and energy band bending to explain the possible mechanism of electrical transport characteristics when ZnO nanowires are bent for bottom-gate ZnO nanowire FETs (a and b) and top-gate ZnO nanowire FETs (c and d). E_V, E_F and E_C are valance band minimum, Fermi level, and conduction band maximum, respectively.

of electrons has decreased, whereas the decrease of transconductance in the top-gate FET suggests the increase of trapped electrons.[24] The results of the transconductance change indicate that bending the nanowire significantly influences the gating efficiency.

The opposite electrical transport behaviors for two different device structures when the substrate and nanowire are bent in various bending curvatures can be explained by the piezoelectric effect and the trapping of electrons at the interfaces between the ZnO nanowire and polymer dielectric, as illustrated in Figure 5. Previously, Wang et al. reported that the piezoelectric effect can influence the electronic transport characteristics of the ZnO nanowires even without any external gate bias.[16] The change of the I_{DS}–V_{DS} characteristics of the bent ZnO nanowires is due to the positive charging of the outer stretched surface (positively strained) and the negative charging of the inner compressed surface (negatively strained) of the ZnO nanowires, both of which are induced by the piezoelectric effect, $E_{PZ} = \varepsilon/d$, where E_{PZ} is the electric field produced by the piezoelectric effect along the nanowire, ε is the strain, and d is the piezoelectric coefficient.[25] This effect results in reduction of the effective channel area through the trapping of the electrons on the positively charged surface and the depletion of the electrons by the negatively charged surface.[16] In addition to the piezoelectric effect, the interface states between the nanowires and the dielectric layers in nanowire FET devices play an important role in electronic transport.[26] The electron trapping at the interface states builds up the depletion region inside the nanowire and results in decreasing the effective channel area and creating the surface potential barrier Φ_s between the nanowire and the polymer dielectrics.

In our experiments, the ZnO nanowire already has a depletion region due to the trapping of electrons at the interface states, and as the ZnO nanowire FETs are bent (Fig. 5a and c), the electron trapping at the interface states is influenced by the different charged surfaces induced by the piezoelectric effect, resulting in a change in the transport characteristics.

Before the nanowire FETs are bent, the energy band bends upward and Φ_s is formed (dashed lines in Fig. 5b and d) due to the electron trapping effect at the interfaces.[26b,27] When the ZnO nanowire FETs are bent by an external force, the strain applied to the substrates is also applied to the ZnO nanowires, causing deflection of the nanowires. From this deflection, the piezoelectric effect-induced potential Φ_{PZ} is created by the relative displacement of Zn^{2+} with respect to O^{2-}.[15b,28] The effect of the Φ_{PZ} on the original Φ_s causes the variation of the effective potential barrier Φ_{eff} at the interface by reducing or increasing the electron trapping, and influences the electronic transport properties of the ZnO nanowire FETs. The bottom side (compressed side) of the ZnO nanowire exhibits a negatively charged surface, which decreases the trapping of electrons by repulsing them away. However, the positively charged surface on the top side (stretched side) of the ZnO nanowire draws and traps more free electrons.[28] For the bottom-gate FET (Fig. 5b), the negatively charged surface causes more electrons to be released from the original interface states, resulting in the decrease of the surface potential barrier at the bottom surface of the nanowire, and the energy band moves downward (i.e., $\Phi_s > \Phi_{eff}$). Therefore, further bending of the nanowire FETs increases the carrier concentration in the channel area, the transconductance, and the current with the V_T shift in the negative gate bias direction. However, for the top-gate FET (Fig. 5d), the additive trapped free electrons by the positively charged surface increase the surface potential barrier at the top surface of the nanowire and the energy band moves upward (i.e., $\Phi_s < \Phi_{eff}$). Therefore, the carrier concentration in the channel area, the transconductance, and the current are decreased with the V_T shift in the positive gate bias direction. The effective barrier height Φ_{eff} is related to the depletion width (W) on the bottom side or top side of the nanowire as[11,29]

$$W = \left[\frac{2\varepsilon_{ZnO}\ \phi_{eff}}{e\ N_d}\right]^{1/2} \tag{4}$$

where e is the electronic charge, N_d is the doping density, and ε_{ZnO} is the dielectric constant of ZnO. The change in W (change in channel area) in relation with Φ_{eff} can explain the current change and V_T shift.

In order to determine whether the aforementioned bending effects of ZnO nanowire flexible FETs are really due to

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piezoelectricity, we performed similar bending experiments using In_2O_3 nanowires that are not piezoelectric materials. Bottom-gate In_2O_3 nanowire FETs were fabricated on PET plastic substrates via the same method as bottom-gate ZnO nanowire FETs on PET substrates. The detailed synthesis process and characterization of In_2O_3 nanowires can be found elsewhere.[30] The representative characterization results are summarized in Figure 6. Figure 6a shows the I_{DS}–V_{DS} characteristics without bending the device and Figure 6b displays the I_{DS}–V_G characteristics when the substrate and In_2O_3 nanowire were bent. Figures 6c and d show the variation of the threshold voltage, mobility, and carrier concentration for four different bending conditions. In addition, top-gate In_2O_3 nanowire FETs were also fabricated on PET plastic substrates via the same method as top-gate ZnO nanowire FETs. The characterization results were similar to the case of bottom-gate In_2O_3 nanowire flexible FETs (data not shown here). These results indicate that there is no distinct tendency of the bending effect in terms of current change and threshold voltage shift in In_2O_3 nanowire flexible FETs, unlike in the cases of ZnO nanowire flexible FETs (Figs. 3 and 4). These differences in the electronic transport characteristics of In_2O_3 and ZnO flexible nanowire devices are because In_2O_3 has no conspicuous piezoelectric property, as ZnO has, and therefore no piezoelectric and bending effect are observed in In_2O_3 nanowires.

In summary, bottom-gate and top-gate ZnO nanowire FETs using polymer dielectrics on plastic substrates were fabricated and investigated while the FETs were bent with various strains. We demonstrated that the piezoelectric effect on ZnO nanowires induced by bending their flexible substrate influenced the electrical transport characteristics of ZnO nanowire FETs in terms of current levels, transconductance, mobility, and threshold voltage. The opposite bending phenomena between the bottom-gate and top-gate structures of ZnO nanowire flexible FETs can be explained by the piezoelectric effect with the electron trapping effect at the interfaces between the nanowire and polymer dielectrics.

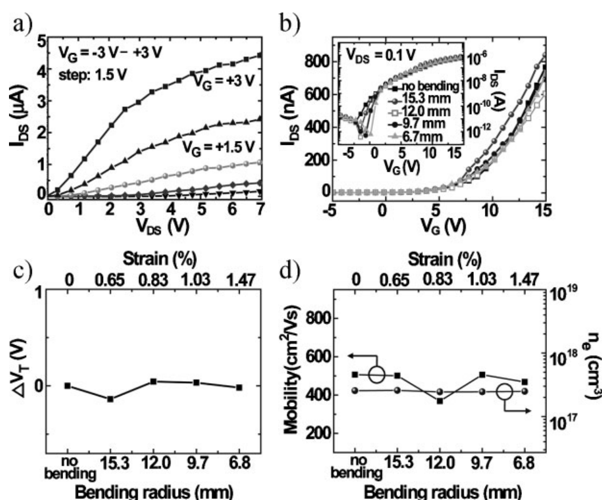

Figure 6. Transistor characteristics of a bottom-gate In_2O_3 nanowire FET on a plastic substrate when the nanowire and substrate were bent with four different bending conditions. a) I_{DS}–V_{DS} characteristics measured for different gate biases when the nanowire was not bent. b) I_{DS}–V_G characteristics when the nanowire was bent. Inset plot is in the semilogarithmic scale. c) Threshold voltage and d) mobility and carrier concentration (at $V_G = 10$ V) as a function of bending radius.

Experimental

Nanowire Growth: ZnO nanowires were grown on *c*-plane sapphire (c-Al_2O_3) substrates by thermally vaporizing a mixed source of commercial ZnO powder (99.995%) and graphite powder (99%) in a ratio of 1:1 in a tube furnace. The cleaned sapphire substrate was deposited with a 3 nm thick Au layer and loaded into the center of the quartz tube with source materials. Then ZnO nanowires were grown on the substrate surface at a temperature of 920 °C for ~30 min under the flow of a gas mixture of Ar at 50 sccm and O_2 at 0.2 sccm.

Device Fabrication and Characterization: The ZnO and In_2O_3 nanowire flexible FETs were fabricated on a PET substrate. First, to minimize the structural distortion of the polymer layer and PET substrate during the process, especially for the curing of cross-linked PVP at 200 °C, the PET substrate was preshrunk at 180 °C for 10 hours to secure a sufficient structural stability [31]. Then the substrate was cleaned with acetone, ethanol, and deionized water. The ZnO nanowire FET devices were fabricated as two different types of device structures: bottom-gate FET and top-gate FET device structures. For the bottom-gate ZnO nanowire FETs, the global bottom-gate electrodes consisting of Ti (10 nm)/Au (50 nm) were deposited by an electron beam evaporator using a metal shadow mask, and then cross-linked PVP (acting as a dielectric layer) was coated on the prepared substrate, followed by a curing step. The cross-linked PVP dielectric layer was prepared by PVP (10 wt% of solvent) mixed with additive poly(melamine-*co*-formaldehyde) methylated (5 wt% of solvent) in propylene glycol monomethyl ether acetate (PGMEA) [22]. The solution was stirred more than 24 hours and then deposited by spin-coating. It was then baked at 110 °C for 3 min and cured at 200 °C for 10 min using a hot plate. The curing step enables the PVP to be cross-linked, which is caused by poly(melamine-*co*-formaldehyde) methylated additive, making the PVP film robust against exposure to other chemical solvents, such as acetone and photoresist [22,31]. The grown ZnO nanowires were then dispersed in ethanol by brief sonicating for 30 to 60 s and placed on the prepared substrate coated with a cross-linked PVP layer by dropping the ethanol solution containing nanowires. The source and drain electrodes consisting of Ti (90 nm)/Au (40 nm) were deposited by an electron beam evaporator followed by a photolithography and lift-off process. The distance between the source and drain electrodes is typically ~5 μm. Finally, the devices were passivated with PVP (10 wt%) dissolved in IPA. For the top-gate ZnO nanowire FETs, cross-linked PVP was prepared on the PET substrate, which increases the adhesion of the S/D electrodes to the substrate. ZnO nanowires were then cast on the cross-linked PVP layer followed by patterning the source and drain electrodes in the same method as the bottom-gate FETs. The devices were spin-coated at 1500 rpm with a PVP polymer dielectric. PVP for the top gate dielectric layer was prepared by PVP (10 wt%) in IPA followed by overnight stirring to ensure that the polymer dissolved completely in the solvent. After baking the PVP top layer at 70 °C for 2 h to remove the solvent, the top-gate electrodes were made by depositing a 50 nm thick Au layer on the PVP layer by the electron beam evaporator. The current–voltage (*I*–*V*) measurements of the fabricated devices were carried out using a semiconductor parameter analyzer (HP4155C). The bending measurement was performed by a simple equipment setup as shown in Figure 1d with various bending radii.

Received: March 11, 2008
Revised: June 19, 2008
Published online: October 9, 2008

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